Jingyu Pan

jingyu.pan@duke.edu / Google Scholar / LinkedIn

Research Interests

Electronic Design Automation (EDA), Machine Learning, Large Language Models.

Education

Duke University *Sept. 2020 - Jul. 2025 (expected)*

- Ph.D. candidate in Electrical and Computer Engineering (Advisor: **Prof. Yiran Chen**)

Zhejiang University *Sept. 2016 - Jun. 2020*

- B.Eng. in Information Engineering

Experience

Computational Evolutionary Intelligence Lab, Duke University *Aug. 2020 - Present*

Graduate Research Assistant. (Advisor: **Prof. Yiran Chen**)

- **AutoML for Digital VLSI Design** [ICCAD'21] [ASPDAC'23] [TCAD'23]
  - Proposed an automated machine learning approach combining feature selection and neural architecture search (NAS) to create routability prediction and analog placement prediction models without human intervention.
  - Achieved a 10% performance gain compared to state-of-the-art manually-designed models while drastically reducing development time to only 0.3 days.
- **Federated Learning for Privacy-Preserving EDA** [DAC'22]
  - Designed a federated learning framework that enables collaborative ML model training for routability estimation while preserving circuit design privacy across multiple clients/companies.
  - Proposed a specialized neural network (FLNet) with personalization techniques that achieved 11% higher accuracy than individual local models, approaching the performance of centralized training without data sharing.
- **Robust ML for VLSI Security** [ICCAD'22]
  - Proposed a novel DRC-guided curvature regularization technique to defend ML-based lithography hotspot detectors against adversarial attacks in VLSI design flows.
  - Decreased attack success rate by 53.9% and improved model accuracy by 12.1% ROC-AUC compared to vanilla models, outperforming conventional defense methods.

Synopsys Inc. *Sept. 2024 - Apr. 2025*

Technical Intern.

- **LLM-driven VLSI Parameter Optimization** [Submitted to ICCAD'25]
  - Developed CROP, the first large language model-powered framework for automatic parameter tuning in VLSI design flows using retrieval-augmented generation.
  - Achieved 9.9% reduction in power consumption compared to state-of-the-art baselines by leveraging semantic understanding of circuit designs and knowledge transfer between similar designs.

Synopsys Inc. *Aug. 2023 - Jan. 2024*

Technical Intern.

- **LLM-based Technology File Generation**
  - Developed a fine-tuned language model system that automatically generates semiconductor technology files from design rule manuals (DRMs), reducing reliance on manual coding by technical experts.
  - Implemented specialized data annotation techniques that dramatically improved numerical value prediction accuracy by creating mappings between rule descriptions and technology file syntax, successfully validating the approach on industrial 65nm and 45nm nodes.

NXP Semiconductors *May 2022 - Aug. 2022*

Research Intern.

- **IR Drop Estimation via Machine Learning**
  - Developed a machine learning pipeline that enables fast IR drop estimation for static timing analysis, drastically reducing computational overhead compared to traditional simulation-based approaches.
  - Conducted feature engineering to extract relevant power grid parameters.
  - Evaluated multiple regression and neural network models to optimize estimation accuracy, achieving good correlation with sign-off tools.

Inst. of VLSI Design, Zhejiang University *Aug. 2020 - Jun. 2021*

Research Assistant. (Advisor: **Prof. Cheng Zhuo**)

- **Heterogeneous Federated Learning for Lithography Hotspot Detection** [ASP-DAC'22] [TCAD'23]
  - Developed a privacy-preserving federated learning framework with local adaptation mechanisms for non-IID data across semiconductor design houses, including an automatic feature selection method to reduce computational overhead.
  - Achieved 7-11% accuracy improvement over state-of-the-art methods with 5× faster convergence, while reducing computational costs by 18.75% during hotspot detection.

Temasek Laboratories, Nanyang Technological University *Jul. 2018 - Oct. 2018*

Research Assistant. (Advisor: **Dr. Shivam Bhasin** and **Prof. Fan Zhang**)

- **Persistent Fault Analysis** [DATE'19]
  - Conducted comprehensive analysis extending Persistent Fault Analysis to evaluate its effectiveness against masking countermeasures, demonstrating vulnerability at any order with merely one single fault injection.
  - Developed statistical models to quantify attack complexity and validated security vulnerabilities in multiple state-of-the-art masked implementations through experimental testing on public cryptographic implementations.

PUBLICATIONS

First Author Papers

[1] **CROP: Circuit Retrieval and Optimization with Parameter Guidance using LLMs.**
*Submitted to IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**). 2025.*

[2] **A Survey of Research in Large Language Models for Electronic Design Automation.** [pdf]
*In ACM Transactions on Design Automation of Electronic Systems (**TODAES**). 2025.*
Jingyu Pan, Guanglei Zhou, Chen-Chia Chang, Isaac Jacobson, Jiang Hu, and Yiran Chen.

[3] **EDALearn: A Comprehensive RTL-to-Signoff EDA Benchmark for Democratized and Reproducible ML for EDA Research.** (Invited Paper) [pdf]
*In Proceedings of the 43rd IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**). 2024.*
Jingyu Pan, Chen-Chia Chang, Zhiyao Xie and Yiran Chen.

[4] **Lithography Hotspot Detection Based on Heterogeneous Federated Learning with Local Adaptation and Feature Selection.** [pdf]
*In IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**). 2023.*
Jingyu Pan, Xuezhong Lin, Jinming Xu, Yiran Chen, and Cheng Zhuo.

[5] **Robustify ML-Based Lithography Hotspot Detectors.** [pdf]
*In Proceedings of the 41st IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**). 2022.*
Jingyu Pan, Chen-Chia Chang, Zhiyao Xie, Jiang Hu, and Yiran Chen.

[6] **Towards Collaborative Intelligence: Routability Estimation Based on Decentralized Private Data.**
*In Proceedings of the 59th Design Automation Conference (**DAC**). 2022.* [pdf]
Jingyu Pan, Chen-Chia Chang, Zhiyao Xie, Ang Li, Minxue Tang, Tunhou Zhang, Jiang Hu, and Yiran Chen.

[7] **Lithography Hotspot Detection via Heterogeneous Federated Learning with Local Adaptation.**
*In Proceedings of the 27th Asia and South Pacific Design Automation Conference (**ASP-DAC**). 2022.* [pdf]
Jingyu Pan, Xuezhong Lin, Yiran Chen, Jinming Xu, and Cheng Zhuo.

[8] **Automatic Routability Predictor Development Using Neural Architecture Search.** [pdf]
*In Proceedings of the 40th IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**). 2021.*
Jingyu Pan, Chen-Chia Chang, Tunhou Zhang, Zhiyao Xie, Jiang Hu, Weiyi Qi, Chun-Wei Lin, Rongjian Liang, Joydeep Mitra, Elias Fallon, and Yiran Chen.

[9] **One Fault is All it Needs: Breaking Higher-Order Masking with Persistent Fault Analysis.** [pdf]
*In 2019 Design, Automation & Test in Europe Conference & Exhibition (**DATE**). 2019.*
Jingyu Pan, Fan Zhang, Kui Ren, and Shivam Bhasin.

Co-Authored Papers

[1] **PRICING: Privacy-Preserving Circuit Data Sharing Framework for Lithographic Hotspot Detection.** [pdf]
*In Proceedings of the 30th Asia and South Pacific Design Automation Conference (**ASP-DAC**). 2025.*
Chen-Chia Chang, Wan-Hsuan Lin, **Jingyu Pan**, Guanglei Zhou, Zhiyao Xie, Jiang Hu, and Yiran Chen.

[2] **Toward Fully Automated Machine Learning for Routability Estimator Development.** [pdf]
*In IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**). 2023.*
Chen-Chia Chang, **Jingyu Pan**, Zhiyao Xie, Tunhou Zhang, Jiang Hu, and Yiran Chen.

[3] **PANDA: Architecture-Level Power Evaluation by Unifying Analytical and Machine Learning Solutions.** [pdf]
*In Proceedings of the 2023 IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**). 2023.*
Qijun Zhang, Shiyu Li, Guanglei Zhou, **Jingyu Pan**, Chen-Chia Chang, and Yiran Chen.

[4] **Fully Automated Machine Learning Model Development for Analog Placement Quality Prediction.** **[Best Paper Nomination]** **[pdf]**
*In Proceedings of the 28th Asia and South Pacific Design Automation Conference (**ASP-DAC**). 2023.*
Chen-Chia Chang, **Jingyu Pan**, Zhiyao Xie, Yaguang Li, Yishuang Lin, Jiang Hu, and Yiran Chen.

[5] **Rethink Before Releasing Your Model: ML Model Extraction Attack in EDA.** **[Best Paper Award]** **[pdf]**
*In Proceedings of the 28th Asia and South Pacific Design Automation Conference (**ASP-DAC**). 2023.*
Chen-Chia Chang, **Jingyu Pan**, Zhiyao Xie, Jiang Hu, and Yiran Chen.

[6] **DEEP: Developing Extremely Efficient Runtime On-Chip Power Meters.** **[pdf]**
*In Proceedings of the 41st IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**). 2022.*
Zhiyao Xie, Shiyu Li, Mingyuan Ma, Chen-Chia Chang, **Jingyu Pan**, Yiran Chen, and Jiang Hu.

[7] **The Dark Side: Security and Reliability Concerns in Machine Learning for EDA.** **[pdf]**
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. 2022.
Zhiyao Xie, **Jingyu Pan**, Chen-Chia Chang, Jiang Hu, and Yiran Chen.

[8] **Pre-Placement Net Length and Timing Estimation by Customized Graph Neural Network.** **[pdf]**
*In IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**). 2022.*
Zhiyao Xie, Rongjian Liang, Xiaoqing Xu, Jiang Hu, Chen-Chia Chang, **Jingyu Pan**, and Yiran Chen.

Honors & Awards

Best Paper Award of the 28th IEEE/ACM ASP-DAC	*Jan. 2023*
Best Paper Nomination of the 28th IEEE/ACM ASP-DAC	*Jan. 2023*
The Second Prize of the 12th National College Student Information Security Contest	*Aug. 2019*
The First Prize of Zhejiang Physics Competition for College Students, 2017	*Jan. 2018*
The First-Class Scholarship for Outstanding Merits, 2016-2017 (3%)	*Sept. 2017*

Skills

Programming	C, C++, Verilog, Python, Bash, TCL
Deep Learning Toolkits	PyTorch, TensorFlow, HuggingFace
VLSI Tools	Synopsys Fusion Compiler, Cadence Innovus, Virtuoso